

XILINX: FPGAs AND SOFTWARE DEVELOPMENT TOOLS

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WEB. <http://www.xilinx.com/>**Q. First of all, tell us a little bit about yourself and your role at Xilinx.**

- A. I've been in the EDA/Silicon industry for more than 19 years. For the past two and a half years I've been responsible for the marketing of Xilinx Embedded and DSP tools, IP and partnerships. In July of this year, I took over as Senior Marketing Director for the Xilinx *ISE Design Suite*, which added the ISE Foundation development tool suite and connectivity IP to my marketing responsibilities.

Prior to Xilinx, I was Vice President of Marketing and International Sales for AccelChip (acquired by Xilinx), group director of marketing for Mentor Graphic's synthesis technologies and Vice President of Marketing for Exemplar Logic. I have also served as a Product Marketing Manger, Technical Marketing Engineer, Account Manager, and Senior Field Application Engineer elsewhere within the EDA industry.

Q. Xilinx is known, obviously, as a leader if not "the" leader in the FPGA space. Before we turn to development tools, can you outline the Xilinx FPGA offerings very briefly?

- A. Xilinx FPGAs fall into two categories; the *Virtex*[®] series of high-performance FPGAs and the low-cost *Spartan*[®] series of FPGAs which targets high volume applications.

The *Virtex-5* family is the fifth generation in the award-winning *Virtex* series. Built upon the industry's most advanced 65nm triple-oxide technology, breakthrough new *ExpressFabric*[™] technology and proven *ASMBL*[™] (Advanced Silicon Modular Block) architecture, the *Virtex-5* family includes five domain-optimized platforms for high-speed logic, digital signal processing (DSP), embedded processing and serial connectivity applications.

The *Virtex-5* family's five distinct platforms gives designers the most choice offered by any FPGA family. Each platform contains a different ratio of features to address the needs of a wide variety of advanced logic designs. In addition to the most advanced, high-performance logic fabric, *Virtex-5* FPGAs contain many system-level hard-IP blocks, including powerful 36-Kbit block RAM/FIFOs, second generation 25 x 18 DSP slices, *SelectIO*[™] technology with built-in digitally controlled impedance, *ChipSync*[™] source-synchronous interface blocks, system monitor functionality, enhanced clock management tiles with integrated DCM (Digital Clock Managers) and phase-locked-loop (PLL) clock generators, and advanced configuration options.

Additional platform- dependant features include power-optimized high-speed serial transceiver blocks for enhanced serial connectivity, *PCI Express*[™] compliant integrated Endpoint blocks, tri-mode Ethernet MACs (Media Access Controllers), and high-performance *PowerPC*[®] 440 microprocessor embedded blocks. These features allow designers to build the highest levels of performance and functionality into their FPGA-

based systems to offer a programmable alternative to custom ASIC technology. Customers can use Xilinx *EasyPath* FPGAs to achieve significantly lower unit costs for volume production once their design is fixed and no longer requires the full programmability of standard *Virtex* FPGAs.

The Extended *Spartan®-3A* family of Field-Programmable Gate Arrays (FPGAs) solves the design challenges for many high-volume, cost-sensitive electronic applications. With 12 devices ranging from 50,000 to 3.4 million system gates, the *Spartan-3A* family provides a broad range of densities and package options, as well as integrated DSP MACs to deliver lower total system costs when compared to alternative solutions. The low-cost family also includes the non-volatile *Spartan-3AN* devices, which combine leading-edge FPGA and Flash technologies to provide a new evolution in security, protection and functionality, ideal for space-critical or secure applications.

The Extended *Spartan-3A* family improves system performance and reduces the cost of configuration. These enhancements, combined with proven 90nm process technology, deliver more functionality and bandwidth per dollar than ever before, setting a new standard in the programmable logic industry. Because of its exceptionally low cost, the Extended *Spartan-3A* family is ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment.

Q. Many surveys, including our own, indicate that software development tools are a critical factor in the “FPGA design experience.” What sorts of FPGA development tools does Xilinx offer? In particular what does one get with “ISE Design Suite 10.1?”

A. The *ISE™ Design Suite 10.1*, the latest release, delivers the perfect combination of design performance and productivity. Whether your design requires a flexible embedded processing solution, a specialized flow for DSP development, or just optimal high-performance logic, the *ISE Design Suite 10.1* can be configured to achieve your design goals quickly.

The *ISE Design Suite* combines the Xilinx Design Tools and IP for Embedded, DSP, and Logic design. This includes the following individual products:

- *ISE™ Foundation™ Software*
- *ISE Foundation Software with the ISE Simulator*
- *Platform Studio and the Embedded Development Kit (EDK)*
- *PlanAhead™ Design and Analysis Tool*
- *ChipScope™ Pro Tool*
- *ChipScope Pro Serial I/O Toolkit*
- *System Generator for DSP*
- *AccelDSP™ Synthesis Tool*
- *CoreGen tool and LogicCore IP*

Q. Can an engineer try these before committing to use Xilinx? In what ways can the development tools be used to “try” before “buying” Xilinx silicon?

A. Xilinx makes it easy to evaluate our world-class FPGA, DSP and Embedded Processing system design tools in the *ISE Design Suite*. If the customer is looking at Xilinx for the

first time or considering additional ISE Design Suite products for their FPGA design environment, a free, downloadable 60-day evaluation gets you started quickly.

In addition, Xilinx offers ISE® *WebPACK*™ software. This is the ideal downloadable solution for FPGA and CPLD design offering HDL synthesis and simulation, implementation, device fitting, and JTAG programming. ISE *WebPACK* provides the tools and features along with the same easy-to-use design environment as our award winning ISE *Foundation*™ design tools providing instant access to the ISE features and functionality at no cost.

Q. What about third party FPGA tools? What companies in that space are prominent partners of Xilinx?

- A. Xilinx has a host of 3rd party partners we work closely with. Because our devices can be used in signal processing, embedded, logic and system level solutions we work with many companies to provide a whole product solution.

For example in the embedded space, we work with 3rd parties such as Agilent, GreenHills, Mentor Graphics, Lauterbach, LynuxWorks, Wind River Systems and others to provide integrated SW development solutions.

In the area of DSP, we partner with, The MathWorks, Synplicity (Synopsys) and National Instruments.

Finally, to provide comprehensive RTL solutions we work closely with Cadence, Mentor Graphics, Synopsys and others to provide verification solutions and with Mentor Graphics and Synopsys (Synplicity) for synthesis. In addition we work with several ESL partners to provide high-level design options to our customers.

Q. One of the most confusing issues in the development tools area is comparing and contrasting the “free” tools offered by vendors like Xilinx and the “paid” tools offered by third party vendors. Where do you see the role of each? Where is there overlap?

- A. Many Xilinx customers use a combination of our *ISE Design Suite* and tools from EDA vendors. However, because of the diversity in the Xilinx customer base, where we work with all sizes of companies, we see those that can afford and want to take advantage of EDA tools and startups that cannot. For those with very tight budgets we feel it is important to offer a comprehensive and integrated flow into our devices. However, for those that can afford it, we encourage customers to leverage whatever third party tool they wish to use in combination with ours.

As for the roles of each, Xilinx views parts of our solution as “core” to Xilinx; for example the map, place and route technology found in ISE Foundation. With the different ratio of features in our silicon to address the needs of a wide variety of logic designs and integrated IP, this technology is critical to our goal of offering the highest performance and lowest cost devices to our customers. Advancements in this technology such as SmartCompile and SmartGuide have enabled customers to cut compile times, resulting in more design iterations per day which is very important considering that we deliver the industry’s largest FPGAs.

As our devices have grown over the years, so has the need for physical synthesis, this is why we also invest in our XST synthesis tool, providing tighter linkages from VHDL or Verilog to the end device. However, many companies do use a combination of XST, Synopsys/Synplicity and Mentor Graphics. The reason behind this is that with any one

design, synthesis results will vary, by trying two or three tools there is the possibility of getting a higher performing design or one with lower area depending on the design goals.

We also see our *CoreGen* tool offered in the *ISE Design Suite*, which we use to deploy the vast IP offerings from Xilinx, as a core technology for us. Because Xilinx offers more than 200 IP cores, it is imperative that we provide an easy to use delivery tool so that customers can rapidly take advantage of our IP.

Another “core” example is *Platform Studio*, which is part of our Embedded Development Kit. Platform Studio enables rapid integration of the more than 60 embedded IP cores available in support of the *MicroBlaze* and embedded PPC405/440 processors. In addition, Platform Studio enables the software drivers needed by software developers. Software developers then can use our Eclipse based IDE, Platform Studio-SDK, or choose a third party IDE to develop code.

In the area of “critical” tools for Xilinx, or tools that we provide to fill gaps in what is available in the market, we provide tools like *ChipScope Pro*, which inserts logic analyzer, bus analyzer, and virtual I/O low-profile software cores directly into a design, allowing users to view any internal signal or node, including embedded hard or soft processors. With *ChipScope Pro* we interface with Agilent bench test equipment. This synchronizes the *ChipScope Pro* tool to Agilent's FPGA Dynamic Probe scope option. This unique partnership between Xilinx and Agilent gives deeper trace memory, faster clock speeds, more trigger options, all using fewer pins on the FPGA. We are also working with embedded trace companies to leverage this technology into the software debug world.

Also in the critical bucket, are our DSP tool offerings, *AccelDSP* and *System Generator for DSP*. Several years ago, Xilinx noticed that there were great tools from The MathWorks (*MATLAB* and *Simulink*) for DSP algorithm design and verification, but they lacked a path into implementation on FPGAs. To enable a rapid path to implementation Xilinx partnered with The MathWorks and released *System Generator*, which leveraged the Simulink environment and married it with our DSP IP to provide an integrated DSP development environment. About three years ago, Xilinx acquired AccelChip, enhanced this offering with *AccelDSP* a MATLAB based algorithmic synthesis tool. Today Synplicity and The MathWorks also offer tools in this space, but when we started out, Xilinx was the only vendor.

In the area of RTL simulation, Xilinx provides *ISE Simulator* to address the cost sensitive market. We however work with all the EDA companies providing simulation technology to provide customers more comprehensive environments over what we offer.

Finally, the third category is what we call “context”. Tools we look to the EDA companies to provide. A great example of this is our ESL initiative where we work with many of the C to Gates companies to providing flows that we are not. In summary, our goal is to ensure customers targeting our devices have complete comprehensive solutions and to foster the ecosystem around tools and IP.

- Q. One of the critiques about the FPGA vendor tools from Xilinx and Altera is that they, allegedly, result in “vendor lock-in?” What are your feelings about “lock in?”**
- A. IP is critical to customers' time to market. Xilinx invests heavily in this area to provide soft and hard IP for connectivity, wireless, video, DSP, embedded and other standards. The reason we invest here is to provide highly optimized cores that provide the best quality of results in our devices to save our customers time and money.

Because many of our tools are built around our IP, for example in DSP and the embedded space, customers may feel that they are locked in, but in the same respect, they are increasingly using our IP because of demands placed on their businesses such as cost,

CAPX, OPEX and schedule pressures. If they choose not to use IP they have the choice to move between vendors, however this may come at a cost of larger less efficient designs and slower time to market. This is just the nature of FPGA architectures and is very analogous with the embedded space where moving between processors is difficult if you have invested in assembly code.

- Q. Another critique is that choosing Xilinx- or Altera-based tools, first, means that the developer is choosing silicon first rather than using independent development tools to identify the “best” silicon for the design, and then choosing this “best” silicon. What is your response to this objection?**
- A. It is difficult to choose the “best silicon” without looking at the total solution. The best solution is a combination of tools, IP, reference platforms and silicon features. Without this combination, the company evaluating an FPGA cannot get a real feel how there design will perform and at what cost. On simple designs it might be possible just to use a vendor independent RTL synthesis tool, however most designs leverage different many aspects of the ISE Design Suite to complete the design. We encourage the use of non-Xilinx point tools in this flow, however no one 3rd party vendor independent company is providing the breath of solution needed for customers to really evaluate what is the best silicon for the design.
- Q. Thank you for this interview.**