

INSIDERS' GUIDE: FPGAs, TOOLS, AND BOARDS



FEATURED INTERVIEW:

EXCERPTED FROM WWW.EG3.COM



Prepared by:

eg3.com

Jason McDonald, Senior Editor

eg3.com

tel: 510.713.2150

email: info@eg3.com

web: <http://www.eg3.com>



TARAY: NEW TECHNOLOGIES FOR FPGA BOARD DESIGN

24 October 2008: FPGA Board Design

INTERVIEWEE. JOE GIANELLI

VICE PRESIDENT MARKETING & BUSINESS DEVELOPMENT

TEL. 408-705-2773

EMAIL. joe@tarayinc.com

COMPANY. TARAY

WEB. <http://www.tarayinc.com/>**Q. First of all, tell us a little bit about yourself and your responsibilities at Taray?**

A. I'm a sales and marketing professional serving the EDA market for the past 20+ years at companies like Cadence, EPIC Design, Synopsys and Synplicity. I'm responsible for the marketing and sales at Taray Inc. Since most of our sales will come from indirect channels, I'll be managing our channel partners too.

Q. It seems that a very special focus of Taray's is the challenges presented by FPGA / board integration. Can you share with us what design challenges you address?

A. FPGA pin assignments affect more than just the FPGA. They also have an impact – potentially a bigger one – on the routability of the PCB. From this perspective, one of the biggest challenges is visualizing the PCB topology so that component placement can be used as a constraint during the pin assignment process. Using 7Circuits' PCB-like view of the design, the quality of the pin assignments at a board level is readily apparent. But 7Circuits doesn't just display this information to the user as an afterthought; it actually uses that data to automatically create board-optimized assignments across multiple FPGA's and components. Two other constraints must also be taken into account during the pin assignment process: the electrical rules of the FPGA and the logical relationships of the signals. 7Circuits' synthesis engine considers all three constraints concurrently (PCB topology, FPGA electrical rules, and signal relationships) to automatically create FPGA and board-optimized assignments.

Q. Would you tell us the key product features of your flagship product, 7Circuits?

A. 1) Tight integration with EDA tools and FPGA vendor tools, 2) Automated pin assignments (what we refer to as I/O synthesis), and 3) an ability to raise the level of abstraction in order to improve design productivity. 7Circuits can automatically generate symbols and schematics for use in the PCB design flow and it can communicate with the FPGA vendor's tools. As mentioned above, it also synthesizes pin assignments based on three constraints. The third feature enables designers to focus at an interface level instead of a pin level. That is, 7Circuits' allows the engineer to specify connectivity at a device level as opposed to classic methods that require him to define connectivity at a pin level. This ability to raise the level of abstraction is similar to writing software in C++ instead of machine language. The productivity gains offered by this kind of approach can be significant.

Q. How does your product integrate with the existing FPGA design tools like those from Xilinx or Altera? Does it have any relationship with any standard PCB layout tools?

A. *7Circuits* can read and write ucf and qsf files for communication with tools from Xilinx and Altera. This bi-directional communication is critical in getting a pin assignment that satisfies both the FPGA and the PCB design goals. From a PCB perspective, *7Circuits* creates Cadence DE-CIS (OrCAD), Cadence DE-HDL, and Mentor DxDesigner symbols and schematics in formats native to those applications. In other words we do not use EDIF or some sort of interface; *7Circuits* integrates natively with those tools. *7Circuits* can also re-use existing symbols. This is vital in processes that require engineers to use symbols from a librarian-sanctioned corporate library.

Q. Mentor Graphics, in particular, seems to offer tools that focus not just on FPGA design but on board integration. How does your tool compete with, or complement, the features of the Mentor tool flow?

A. *7Circuits* is integrated with Mentor's DxDesigner schematic capture package. As with Mentor's FPGA/PCB tools, the link between the schematic and the PCB is not affected – there is nothing *7Circuits* does or does not do that affects that link. So *7Circuits* can be used to initiate an FPGA-based system design that will eventually be targeted at DxDesigner and ultimately one of their PCB tools. What separates *7Circuits* from Mentor's product (I/O Designer) is that *7Circuits* creates an optimal set of pin assignments from the outset. I/O Designer takes a 'clean it up later' approach, requiring the team to create a PCB layout first (which implies creating a set of schematics that at a minimum represent FPGA connectivity), then asks the user to manually re-assign pins based on knowledge gleaned from the PCB component placement. *7Circuits* gets around all this through the use of a PCB-like 'canvas', using placement information at the beginning of the design cycle as a constraint in initiating the pin assignment process.

Q. What is your typical customer like? What sorts of target design projects or applications are best served by 7Circuits?

A. We do not have a 'typical' customer; *7Circuits* has been used to create designs with as few as one or two FPGA's to huge systems containing almost 50 FPGA's. These customers range from startups to global, Fortune 50 corporations. *7Circuits* is not vertically oriented – any company creating products containing FPGA's can benefit from *7Circuits*' functionality.

Q. How much does the product cost? What is a typical engagement like? Would you share with us the structure of a typical engagement from the beginning to end?

A. Our *7Circuits* product starts at \$10k and is priced higher for more complex designs. Optional FPGA libraries are also available from Taray starting at \$1.5k. We engage system design teams similar to other EDA vendors, providing an evaluation license based on a mutually agreed evaluation process. Taray works closely with the customer from the outset to establish the evaluation plan and criteria for success. During this process some customers choose to procure the on-site training or design services from Taray to help kick off their use of *7Circuits* in the initial project.

Q. Some of the common questions from your customers might be of interest. For example, what problem are you solving?

A. Despite the growing complexity of FPGAs and their ever-increasing pin counts, system designers, FPGA designers and PCB layout designers are still manually assigning the programmable pins on FPGAs used on PCB designs. This task has become daunting and is

becoming more error prone. Taray's mission is to bring automation to this sorely needed place in the systems designs flow.

Q. So, what exactly is automated?

- A. Taray's *7Circuits* product uses patented I/O synthesis technology that considers three different dimensions to the problem as it optimizes the best pin assignments for all FPGAs associated with the PCB design. The first is the logical integrity of the system design. This includes maintaining the correct protocol interconnections between the FPGAs and other devices such as memory, DSP, processor, or another ASIC. The second is the physical interconnects that *7Circuits* models in a rats nest. In this case, the *7Circuits* technology is minimizing interconnect crossover for the PCB router. The third is the electrical design rules for the I/Os within the FPGAs. *7Circuits* has its own built-in design rule engine, for each FPGA device family, to ensure pin assignments are DRC correct when assigned.

Q. What does the ROI look like for your product?

- A. What we see in typical FPGA based PCB design is that approximately 10% of the overall design effort is spent on assigning and re-assigning the pins for the FPGAs. Since this affects the systems designer, the PCB layout designer, and the FPGA designer, 10% of a 6-month project represents about 4 person months of resources. The *7Circuits* product has been shown to reduce this from a 4-person month job to just 2 weeks, saving the project 3.5 months of effort. In most cases, this labor savings alone pays for the *7Circuits* product in less than 6 months.

Due to the error prone manual process that's in use today, we also see mistakes made on assigning the correct reference voltages or external terminations around FPGAs. Things like this are often not found until the board is fabricated and thus unusable. This wastes weeks of time and PCB manufacturing costs. Using *7Circuits* maintains these connections correctly eliminating this costly error prone step.

Q. Thank you for this interview.