

MENTOR GRAPHICS: VENDOR INDEPENDENCE FOR FPGA DESIGNS

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Q. First of all, tell us a little bit about yourself and your responsibilities at Mentor Graphics.

A. I started my career as a hardware engineer developing hardware for physical modeling at Daisy Systems. I then moved on to technical and management positions with responsibility over EDA tools for programmable devices and for Daisy's proprietary hardware behavioral language. I joined Mentor Graphics in 2005. In the years between Daisy and joining Mentor Graphics, I was in networking, enterprise software, defense and eHealthcare companies. I was also the CEO of Tegrity, an e-Learning company that I founded in the mid-nineties. I held management and executive positions in marketing, engineering, sales and operations for the Israeli Department of Defense, Daisy, Tegrity, Castelle and BackWeb. In addition, I hold patents in image processing applications and won the Israeli Prime Minister Award for product innovation. I am a graduate of the Technion's School of Electrical Engineering, Israel, and hold a master's degree in engineering management from Santa Clara University, CA.

Q. We have only a short space for this interview, but would you please give us a high-level overview to Mentor Graphics' tool solutions that *specifically* address the needs of FPGA-based designs? What is Mentor's design philosophy, and what are the available tools?

A. The prevailing trend of increasing complexity of today's platform FPGA designs while shrinking time-to-market requirements have driven a variety of challenges in design creation, verification, and implementation—and ultimately the need for more ASIC and SoC-like solutions. FPGA designers are turning to higher levels of abstraction, using more efficient design and test languages such as SystemVerilog, relying on internal IP re-use and external IP, and moving to more advanced verification tools and methodologies. For implementation, users are demanding synthesis that meets quality-of-results (QoR) requirements and leading-edge board tools for efficient PCB layout.

We believe that it is critical for FPGA designers to retain the flexibility to retarget their designs to devices from different FGPA vendors. FPGA vendors always leapfrog each other in offering the biggest, fastest, or most power-efficient devices on the market. Hence, designers are looking for methodologies that don't lock them into one FPGA vendor.

Since you asked about Mentor tools in the FPGA space, I believe that we are the clear EDA leader because we are the only company with the complete flow: Design Creation, Verification, Synthesis and PCB tools. The list of Mentor products is too long to mention here, but I'll mention just a few: *Catapult™* and *Vista™* tools allow for high levels of abstraction, *HDL Designer™* allows for efficient design creation, re-use and documentation, and the *Precision®* product family is used for FPGA synthesis. *Precision* is gaining prominence as a leading FPGA synthesis tool and, when used with other Mentor tools, it allows for a complete ESL-to-FPGA

gate flow. Our *Modelsim*® and *Questa*™ products are the leading verification tools for FPGA designers, *FormalPro*™ is our equivalence checking tool, and of course we have a wide range of PCB tools including I/O Designer. We also continue to add more tools to our product portfolio. Lastly, as part of our on-going commitment to mil-aero companies, we are engaged in helping project teams meet DO-254 requirements by providing a complete and consistent tool flow, as well as methodologies, to assure the safety of FPGA devices in airborne systems.

Q. Now, of course, one of the most confusing and important choices for an FPGA design is the choice of tools. Each FPGA vendor has “free” or at least “low cost” tools, yet a few vendors like Mentor Graphics also sell tools into the space. When do you feel vendor-based “free” tools are most appropriate and when do the paid tools like those from Mentor make the most sense?

A. We believe that free vendor tools are not the best choice for companies that are using or planning to use FPGA devices from different vendors. Keep in mind that when one FPGA vendor meets your needs today, another vendor might introduce a new device that is a better choice for your future projects. New FPGA vendors, like Achronix, are coming up with innovative devices that are only supported by commercial EDA providers like Mentor. Commercial EDA tools are vendor neutral and have an advanced feature-set to provide high quality of results, advanced debug, incremental flows, physical synthesis technologies, and rich mixed-language support.

When a complete flow from an EDA company is used, the support and integration are often better because of the single point of support and problem ownership. We do not believe that using free vendor tools saves the customers money because the cost of these tools is often significantly less than the cost of vendor-dependence.

When I was a hardware engineer, and this is still the case today with many customers, I was instructed to do whatever I could to minimize vendor-dependence, so the purchasing manager could use price leverage against vendors, and engineers would always be able to objectively select the best silicon for their projects. Users often call us when they “get stuck” and their project is delayed and at risk of missing the market window. This does not mean that vendor tools should never be used. In fact, choosing a vendor neutral synthesis product as the primary tool means the vendor tool may be kept on reserve. Because synthesis is based on heuristics, no tool will produce the best results for every single design. Lastly, the vendor neutral FPGA synthesis market is over \$80 million, per Gary Smith EDA. I consider this another proof that there is a need for vendor neutrality.

Q. From your experience with customers, do you see a lot of “design reuse” across designs? In what ways does buying into the Mentor tool chain help with design reuse? In what ways do you think using the FPGA vendor tools might not be helpful with design reuse?

A. Almost every customer we speak to makes use of internal and external design reuse – the design community is truly going “green.” The majority of reuse comes from internally created HDL designs or design blocks, and most often they are being reused by engineers unfamiliar with the original design. Main points to enable good design reuse are ensuring: (1) all the design files/references are provided, (2) the quality of the code to be reused is good, and (3) the engineer can quickly understand the design intent of the reused blocks so that he/she can incorporate them into the new design.

Mentor’s *HDL Designer*® product fulfills these steps in an automated way to accelerate design reuse. First, it checks the design integrity to make sure the design blocks to be reused are complete and the coding is legal. Secondly, it assesses the quality of the coding because if the

quality is not high enough, it could be more efficient to code from scratch rather than re-use. That decision should be made early in the design process, before investing too much time. The final step, once the integrity is sound and the quality is high, is to hasten the understanding of the design blocks' functionality via generating visualizations of the HDL code. It's the "a picture is worth a thousand words" concept. It is very difficult and time-consuming to read HDL code and sift through many files in order to understand the full functionality of the code. Viewing FSMs for control logic, block diagrams, or spreadsheets for connectivity, and flow charts for sequential logic is more efficient than scrolling through text files. The visualization also aids in documentation.

IP that is provided by FPGA vendors cannot easily be retargeted to FPGA devices from other vendors. Hence, if your next project fits better in an FPGA from another vendor you will have to spend time retargeting the IP, making design reuse more challenging. If the IP has standard interfaces, this task may not be as difficult. If the IP is a CPU, on the other hand, this task can be painful.

Q. Let's look at "intellectual property" or "IP." Is the story the same here in that the "free" FPGA IP has lock-in issues vs. the IP available from companies like Mentor Graphics? Or are there additional positives to using Mentor Graphics' tools vs. FPGA vendor IP? What about IP designed by the customer himself?

A. "Free" IP provided by FPGA vendors is most certainly part of the vendor lock-in strategy. When users go through the time and effort to integrate a vendor's free PCI core or processor into their design, they are less likely to want to start from scratch with another device—even if it has a superior offering. Hence, adoption of free FPGA IP can become a major obstacle to a truly vendor independent methodology. This is why we recommend turning to device-independent IP companies whose IP can be targeted to any of the major FPGA vendors.

IP designed by the customer, however, is an entirely different matter. Internal IP is under the user's control and usually coded in standard HDL. This typically can be re-targeted to a different FPGA device using a vendor-independent commercial tool.

Q. Again, because we have so little space here, help our readers out by pointing out some of the ways that they can "learn" about Mentor before having to buy. What sorts of available demos, online learning, webinars, etc., does the company offer to FPGA designers?

A. We provide a broad selection of online resources available at <http://www.mentor.com/> including demonstrations for *Catapult C* high-level synthesis, *Precision Synthesis*, *HDL Designer* and other tools. Each product page will have a link to the product's respective online demo.

In fact, Precision Synthesis has recently released a series of webcasts—each of which includes a brief presentation and product demonstration that highlights a specific capability or design methodology, such as advanced synthesis optimizations, incremental design flows, embedded FPGA resource management, and SystemVerilog for design. These on-demand webcasts are available at http://www.mentor.com/products/fpga_pld/events/synthesis_webcast_series.cfm.

Q. Thank you for this interview.