

# INSIDERS' GUIDE: FPGAs, TOOLS, AND BOARDS



## FEATURED INTERVIEW:

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## GATEROCKET: DEVICE NATIVE FPGA VERIFICATION &amp; DEBUG

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**Q. First of all, tell us a little bit about yourself and your responsibilities at GateRocket.**

A. I have been involved in the semiconductor business for 24 years. Initially starting in the test market and moving to the electronic design automation space. I guess that chips are in my blood. I enjoy the fast pace and the continual change since it creates opportunities for creative entrepreneurs. As CEO I am responsible for the leadership of the company, making sure we are focusing in the right areas and ensuring we are paying attention to our customer needs. So long as you are solving a problem for the market and you take the right steps delivering an effective solution, you can build a great company. That is what we are trying to do at GateRocket.

**Q. GateRocket has made a name for itself by “device native” FPGA verification and debug. Can you tell us in just a few short sentences what is meant by “device native” and what is unique about your RocketDrive and RocketVision?**

A. Device Native is the way we describe how our product is different from other products in the market. In addition, our product is focused on Field Programmable Gate Arrays (FPGAs) therefore; Device Native is referring to how we help people verify their designs on these devices. Our solution enables an engineer to see the behavior of their FPGA design running in the actual FPGA chip (the native device) while working in their simulation environment. We have recently blogged about the concept of Device Native verification on our [RocketBlog](#). The benefit is there is no translation, no guesswork. You see what you are going to see in the lab while in your simulation environment. This is very powerful indeed.

**Q. There are of course two to five major FPGA vendors, depending on how you count, and many product varieties at each vendor. How do you support all these devices? Do you support only Xilinx and Altera? Lattice, for example, is not an option? What about specific Xilinx or Altera families - do you support them all?**

A. We have been focused on the large players in the market. According to recent market statistics, Altera and Xilinx own 87% of the FPGA marketplace. We have decided to focus on these two vendors and offer solutions for their most recent FPGA offerings. We are focused on solutions for the largest and most advanced chips. Additionally, we plan to offer RocketDrives for each of their new families of devices as they become available to the general market. For Altera we currently ship a Stratix 2 RocketDrive. I would rather not prematurely announce future products; however the philosophy I described above will apply for their future devices. We recently [announced availability of Xilinx Virtex-5 RocketDrives](#). Of course, we previously announced availability of the Virtex-4 RocketDrive as well. We have not made a decision to support other vendor's devices since we just have not seen the demand for it to date.

**Q. Another big issue is tools. How does your product interface with the tools provided by Xilinx and/or Altera?**

A. We have developed our product to automatically and seamlessly integrate with their tools because that is what our customers own. A key feature of our product is to integrate into our customer's existing environment. In this way we do not disrupt their development methodology or tools, we complement or supplement it by adding significant value in verification and debug. Our founder, Chris Schalick worked as an ASIC designer and later as an FPGA designer. He recalls the frequent times when an EDA vendor would present a new methodology or tool but in order to gain the benefit you needed to change out your existing method or tools. His vision for creating a product that seamlessly fits into existing environments and adds value is realized in the GateRocket product. It is one of the key principals and values we abide by.

**Q. What about third party tools like those from Mentor Graphics? How does your product work with those "independent" tool chains?**

A. We see the great work that Mentor Graphics is doing as critically important to the FPGA development process. In fact each of the major simulation vendors Cadence, Mentor Graphics and Synopsys (alphabetical ordered) is a partner with GateRocket in delivering Device Native verification. It is similar to the question above where the customer has their simulation environment intact. In most cases they do not want to make a change but they have a burning need to find bugs in their FPGA design more quickly or accelerate the overall verification process. We have taken significant steps to ensure that our product works well with the simulation vendor products and supports the new verification methodologies they are promoting. We test our products with the simulators and FPGA vendor tools to ensure our product works well with theirs and delivers our key value points of faster verification and debug for FPGAs.

**Q. Many FPGA designers, if not all, take third party "intellectual property" (IP) as well as their own in-house IP and integrate that into their design, with many headaches about integration and verification. Does GateRocket help with the integration and debug/verification of IP from many sources? How so?**

A. You have hit on a key issue that is facing the FPGA community. This problem is not restricted to FPGA designers; IP has been a long-standing problem for the ASIC market as well. When you purchase any significant IP block, in most cases the documentation alone can be 100 pages or more. This complexity makes it very difficult for an engineer to understand all of the nuances of the IP. What's more, the simulation models the engineer receives generally do not behave identically as the IP in-silicon because they are behavioral models or not as accurate as the actual IP on the chip. In addition, the testing of the IP in many cases is not complete enough to validate all of the configuration options or corner cases. In the end, the designer has difficulty controlling the IP and verifying in a software simulator if it is going to do the right thing in the FPGA. GateRocket enables the engineer to see the behavior of the IP in-silicon while being stimulated with all of the tests they have created in their simulation environment and compare the differences. Since the design goes through the full FPGA synthesis and place and route process they can determine immediately if the IP is operating as desired on the chip. Once complete, the designer has verified that the IP works in-silicon while leveraging their simulation and FPGA vendor tools enhanced by the GateRocket products, cutting weeks out of the system debug process.

**Q. How does a prospective customer engage with GateRocket? In particular, tell us about pre-sales engagement opportunities - like webinars, NDA agreements /**

**demos, and other ways that an engineering team can “test” GateRocket before having to commit to a full financial engagement.**

- A. The best way to engage GateRocket is to contact us by reviewing our [events page](#) on our web site and [registering for a webinar](#) or participating in one of the live trade events. In addition, we offer private demonstrations as well. Each customer has a different requirement for engaging in these types of products. As a start-up we custom tailor our approach to the needs of the customer. In all cases we work to making it as easy as possible to do business with us.

**Q. What questions should an FPGA designer or verification engineer ask themselves to determine if they could benefit from a RocketDrive**

- A. Do they find themselves in the lab with an FPGA that does not work? How long does it take to find each bug in the lab? Are they constraining their use of IP that could otherwise make their company more competitive because of the risk of getting the IP to work? Do they have long simulation times? Are their designs large and complex? There are more but it is best if they are concerned with their FPGA debug productivity to contact GateRocket.

**Q. Thank you for this interview.**