

FPGA SUMMIT: GET YOUR HANDS-ON FPGA EXPERIENCE AT THE SUMMIT

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Q. First of all, tell us a little bit about yourself and how you came to be involved with the inaugural *FPGA Summit*.

A. I've been involved in embedded system design for well over 30 years and have long been interested in FPGAs. Recent advances have led to them being far more than just logic replacement devices, so I thought it was time to have an engineering event dedicated to them. We have put together events in the hardware design area for many years, and this seemed to be a good topic for us now.

Q. What is the “elevator pitch” for the *FPGA Summit*? Tell us a little bit about it. What will one learn there? Who should attend? Where and when is it?

A. FPGAs today provide new tradeoffs between hardware and software. Today's large devices with millions of gates, on-board processors, and high-speed interfaces allow designers to achieve hardware speeds without the costs and complexities of custom design. FPGAs can essentially replace processors in applications such as signal processing, providing acceleration without any new algorithms. Meanwhile, they're even more useful than ever as logic replacement devices, saving space, power, and cost in a variety of applications with devices available for less than a dollar apiece.

The FPGA Summit (<http://www.fpgasummit.com/>) will be at the San Jose Wyndham Hotel in the heart of Silicon Valley (between the 101 and 880) on December 9-11, 2008. It is aimed at hardware design engineers, embedded systems engineers, engineering managers, and communications engineers. It is also for instrumentation and control specialists who may lack such digital background. Attendees will get the latest information on how to use FPGAs in communications, networking, instrumentation, automotive, consumer, military, defense, aerospace, and control applications, including discussions of how to get applications up and running, implement reconfigurable and high-performance computing, get applications done on time, and perform verification. We'll even discuss the great mystery of project time and cost estimation, as well as provide the latest market research and customer experiences. Panel sessions will review the latest developments, provide an opportunity to ask questions in small groups, and cover the key things one needs to know today. Hands-on sessions will cover embedded design with LabVIEW, memory interfacing, and on-board processor usage. And we will have the magic words in Silicon Valley – free parking!

Q. Keynotes are always great events at these sorts of things. Who are the keynote speakers going to be? Any quick bullets on what they will discuss?

A. Keynote speakers will be:

Simon Bloch, VP/General Manager, Design and Synthesis Division, Mentor Graphics on high-level design of FPGAs. He'll describe new ways to handle multi-million gate devices.

Andrew Dauman, VP Engineering, Synplicity Business Group, Synopsys, on increasing productivity for FPGA design groups.

Misha Burich, Sr VP R&D, Altera on achieving higher performance and lower power consumption with FPGAs

Q. FPGAs reach many broad vertical markets, from medical to military. Is there any special vertical focus to the Summit? Are there specific tracks relating to specific applications?

A. We will have specific sessions on communications and networking applications, DSP applications, military/defense/aerospace applications, and low-power applications. We'll also have expert tables on specific vertical areas as part of our special evening Beer, Pizza, and Chat with the Experts session (yes, featuring free beer and pizza).

Q. eg3.com's FPGA Guide has a strong focus not just on FPGAs but on FPGA tools and boards. What aspects of the FPGA summit will touch on tools and/or boards as they relate to FPGA designs?

A. Our hands-on sessions will cover the latest boards from National Instruments and Xilinx. We'll also have special sessions on getting applications up and running and on getting them done on-time and on-budget. We'll have a session on EDA tools and coverage of board-level approaches to defense, instrumentation, and control applications.

Q. Is there an exhibitor showcase or exhibition? If so, what sorts of exhibitors will be there? What days and times will have exhibits?

A. There will be a small exhibit area focused on tools, devices, and accessories. Our sponsors are Mentor Graphics and Synopsys. Other exhibitors include Achronix, Agility, Aldec, Bittware, DefineView, GateRocket, ProDesign, and Taray. Exhibits will be on Wednesday, December 10, from noon to 2 pm and 5 to 7 pm, and on Thursday, December 11, from noon to 2 pm.

Q. Finally, how much does it cost? What is the range of attendance options?

A. Basic cost is \$995 for admission to hands-on sessions, tutorials, and all other events through December 4, and \$1,495 on-site. Discounts are available for exhibitor customers, group members, and college faculty members and students. Exhibit-only registration (for keynotes and many other sessions) is available for free through December 4. One-day registrations are available for hands-On sessions and tutorials for \$495.

Q. Thank you for this interview.