

BLUE PEARL SOFTWARE: VALIDATING TIMING CONSTRAINTS IN FPGAS

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Q. First of all, tell us a little bit about yourself and your responsibilities at Blue Pearl Software.

A. I'm the vice president of marketing at Blue Pearl Software, responsible for product marketing and corporate marketing for the company. I started working in semiconductor design in England and migrated to the United States with National Semiconductor. I worked for a number of small and large semiconductor companies including Product Marketing at LSI Logic before moving to work for EDA companies such as Avanti and Synopsys. I joined Blue Pearl Software over 3 years ago to bring our productivity improving products to market and grow a successful start-up in Silicon Valley.

Q. Most of our readership for this guide is interested in using FPGAs for actual deployment, as opposed to using them for ASIC prototyping. Do your products fit this sort of need? And, of course, could you please just give us a few bullet points about your products and your value proposition for the FPGA community?

A. Blue Pearl Software has 3 products that are integrated into a single executable that allows designers of ASICs and FPGAs to improve their productivity and reduce design time. *Indigo RTL Analysis* is a functional analysis and linting tool that parses RTL descriptions to provide valuable feedback on potential errors for both the design and the design flow. Indigo helps designers write correct RTL quicker.

Cobalt Timing Constraint Generation generates SDC timing constraints from the RTL description to provide the designer with a comprehensive set of accurate constraints to enable faster timing closure. Cobalt saves designers a huge amount of time writing timing constraints and the comprehensive SDC file generated achieves faster implementation of a correct chip.

Azure Timing Constraint Validation reads in the RTL description and the SDC file for that design to automatically validate the timing constraints which significantly lowers the risk to implement a digital design. Azure saves designers a lot of time checking whether they have a correct SDC to use for chip implementation.

Q. As design complexities increase apparently so does the importance of "timing constraints." For those who haven't necessarily thought about this issue head-on, can you explain why "timing constraints" are increasingly important in complex FPGA designs?

- A. FPGA designs are increasingly becoming larger and more complex, like ASIC designs. They often have embedded processors, intellectual property, other pre-existing modules and multiple clocks. These designs increasingly push the limits of area, power, and performance. The fastest timing routes quickly become congested and it gets more difficult to optimize for performance.

Timing constraints, which include clock rates, i/o delays, and timing exceptions are provided to the synthesis and Place & Route tools, to direct them to achieve the necessary timing targets to meet the performance requirements and close timing quickly. For large, complex chips the SDC file can quickly get very large, hundreds of Megabytes to Gigabytes, and designers spend more and more time generating the SDC file and ensuring that it is correct for the design.

Blue Pearl's Cobalt Timing Constraint Generation tool automatically generates the timing exceptions from RTL saving designers many weeks of work and Azure Timing Constraint Validation validates the SDC file against the RTL description to assure the designer that he is using a correct file for chip implementation.

- Q. What solutions does Blue Pearl offer for timing constraints? In the pre-interview back and forth, you mentioned that your *Azure Timing Constraint Validation*TM addressed just this need. Can you tell us about it?**

- A. In addition to *Cobalt Timing Constraint Generation*, which has been on the market for 2 years, Blue Pearl also offers *Azure Timing Constraint Validation*.

Many designers use a system-on-chip (SOC) design methodology and use Intellectual Property (IP) blocks from 3rd party vendors and legacy code from previous generations of designs. That means that they are dealing with RTL descriptions with which they are not familiar and, to get the best performance, they need to check that the constraints they have are correct. *Azure Timing Constraint Validation* is extremely helpful to provide validation of the existing constraints for the legacy and IP blocks that are major chunks of their design.

Azure assures the designer that he is using a correct file for chip implementation, significantly reducing design risk. Designers often write constraints with wild cards, which cover multiple paths in the design. Such a generalized false path constraint can include a path that is not false, and no timing gets reported at timing analysis (STA). This can result in a timing error that could make the design non-functional. Checking these generalized constraints for accuracy is vital to achieving a correct design. *Azure* performs a thorough analysis for all specified paths and provides the designer with a much higher level of confidence in the SDC being used to drive synthesis and Place &Route.

Moreover, as these blocks are integrated into their chip, *Azure* can check that the block level constraints are valid in that chip application. *Azure* can also check the chip level constraints written for that application. *Azure* is our latest tool that we have introduced to the market and can be used by designers using any digital chip design flow.

- Q. Moving upwards a bit, how does your product work with the other software products out there for FPGA design, such as those supplied by the FPGA vendors themselves as well as third party tools chains like those provided by Mentor Graphics, Synplicity/Synopsys, etc.?**

- A. We have partnered with Synplicity/Synopsys and Mentor Graphics to ensure that we understand the SDC that they support. That means that designers can use both *Cobalt* and *Azure* with tools from Synopsys and Mentor. We have also partnered with the major EDA vendors such as Magma to ensure that our tools are integrated with their ASIC flows. We do work with Actel, Altera and Xilinx to be compatible with their design flows as well.

Q. How much do your tools cost? What is the business engagement model?

A. We have an ASIC EDA tool model of pricing for our tools that includes time based and perpetual licensing but have aggressively introduced and offered a 3 month time based license that enable companies to adopt our tools on a project basis. This should be an attractive alternative for FPGA design houses who tend to work with proprietary tool sets.

Q. Since it's a very big commitment to obtain your tools, what do you recommend a potential customer do to "try" before "buying?" Are there webinars, seminars, online learning or white papers? What about pre-sales technical support or trials under NDA? Can you tell us about any pre-sales methods for pre-engaging Blue Pearl?

A. Actually, the level of commitment to obtain our software, is less than you might think. There is almost no learning curve, which means it is easy to bring designers up to speed on how to use each tool and if one designer leaves, his/her replacement can quickly step in and pick them up without difficulty.

Blue Pearl Software tools are priced affordably and integrate with every major design flow. They can be evaluated within a couple of weeks or less. We have demonstrated all of our tools at DAC, ICCAD, and GSA events. We offer Timing Closure seminars on a regular basis to introduce customers to our technology and capabilities. In addition, our website has product descriptions, datasheets, white papers, and customer testimonials.

For customers interested in purchasing our tools, we offer a free, fully supported two-week evaluation period. We also offer extended evaluations and/or project-based licensing for a minimal cost. Customers get a return on their investment in as little as one design.

Q. Thank you for this interview.