

ALTERA: FPGAs AND THE TRANSITION TO 40 NM

1 October 2008: FPGAs and the Transition to 40 nm

INTERVIEWEE. DAVID GREENFIELD,
 SENIOR DIRECTOR OF PRODUCT MARKETING, HIGH-END PRODUCTS
 TEL. 408-544-7000
 EMAIL. catalog@altera.com
 COMPANY. ALTERA
 WEB. <http://www.altera.com/>

Q. First of all, tell us a little bit about yourself and your responsibilities at Altera.

A. I am responsible for Altera's high-density and high-performance *Stratix*[®] product families. I joined Altera in 1995 and have held several management and marketing positions, including director of tools marketing and EDA relations, and manager of target applications. Before joining Altera, I held ASIC marketing, field applications engineering, and design center manager positions with Wyle Electronics, and staff design-engineering positions with Hughes Aircraft. I earned a BS in engineering from Harvey Mudd College, an MS in electrical engineering from University of Southern California, and an MBA from UCLA.

Q. Altera, obviously, is one of the "Big Two" when it comes to the FPGA ecosystem. Can you outline, very briefly, the products that the company provides and your position as a leading FPGA vendor?

A. Altera is the leader in innovative programmable solutions, and has been ever since inventing the world's first programmable logic device in 1983. Altera's solutions address a range of design concerns—from power consumption to performance to cost—for customers in a wide variety of industries, including automotive, broadcast, computer and storage, consumer, industrial, medical, military, test and measurement, wireless, and wireline. In addition to devices, Altera's comprehensive solutions portfolio contains fully integrated software development tools, versatile embedded processors, optimized intellectual property (IP) cores, reference design examples, and a variety of development kits.

The Altera[®] product lines are as follows:

- *MAX*[®] *CPLDs*: Instant-on capability, combined with single-chip, non-volatile, and ease-of-use characteristics in a wide range of packaging options, make *MAX CPLDs* ideal for virtually any digital control function.
- *Cyclone*[®] *FPGAs*: For cost-sensitive, high-volume applications, Altera offers the *Cyclone FPGA* series—the industry's only FPGAs designed from the ground up for low cost. Each series member is optimized individually for cost and delivers a high-volume solution that's competitive with ASICs and ASSPs. The density range for the *Cyclone FPGA* series is 2,910 to 120K logic elements.
- *Arria*[®] *GX FPGAs*: *Arria GX FPGAs* use proven transceiver technology that supports a variety of serial interface protocols such as PCI Express, Gigabit Ethernet, and Serial RapidIO[®], to bridge serial interfaces to legacy parallel interfaces or other serial interfaces. The *Arria GX* family is comprised of five devices ranging in density from 21,580 to 90,220 logic elements.

- *Stratix FPGAs*: Altera's *Stratix* series of high-density, high-performance FPGAs feature unprecedented densities, performance, and low-power leadership. The *Stratix FPGA* series is comprised of devices ranging in density from 10K to 680K logic elements.
- *HardCopy® ASICs*: Through its unique FPGA front-end design flow, *HardCopy ASICs* enable designers to use Altera's *Stratix* series FPGAs to develop, verify, and finalize their system design before committing to production volumes. This unique flow allows designers to deliver their systems to market on average 9 to 12 months sooner than competitors.
- *Quartus® II software*: Altera's *Quartus II* design software is number one in performance and productivity for *CPLD*, *FPGA*, and *HardCopy ASIC* designs.
- *Nios® II embedded processor*: As a 32-bit soft processor core, the *Nios II* offering can be implemented in any of Altera's *FPGA* or *HardCopy ASIC* device families, insulating designers' embedded software investment from processor obsolescence. The proven *Nios II* processor is the most popular configurable soft processor in the industry.
-

Q. Most of our readership are not on the “cutting edge” of FPGAs but rather are practical designers that need to get an FPGA-based design out of the door quickly and efficiently. That said, peel back the curtain a bit, and share with us Altera’s vision of the transition to 40 nm for FPGAs.

A. The move to 40 nm is a significant step for the FPGA industry and this process offers clear benefits over prior nodes, including the 65-nm node and the emerging 45-nm node. With Altera at 40 nm, it's not about sacrificing one benefit to gain another. Altera's 40-nm solutions give designers the benefits of high density, high performance, and low power.

Culminating a multi-year effort of planning, development, and close collaboration with our foundry partner TSMC, Altera's *Stratix IV* and *HardCopy ASIC IV* families enable early and broad access to 40-nm technology that would otherwise be out of reach for many customers. As a result, Altera customers gain access to the most advanced custom logic products delivering the capabilities, performance, density, and power consumption to address the most pressing needs of today's system designers. These parts are on track to ship to customers before the end of this year (2008).

Q. What application areas do you think will be the first to benefit from 40 nm? What sorts of engineers and design companies do you think should really be paying attention?

A. Altera 40-nm devices meet the diverse high-end application needs in a large number of markets such as wireless and wireline communications, military, broadcast, and ASIC prototyping. With the increasing demand for services such as video over Internet, high-speed wireless data, and digital TV, designers must deliver solutions that provide higher data rates, higher interface bandwidths, and increased data processing all in a power-efficient manner. To address these design challenges, Altera is leveraging its innovations in transceivers, memory interfaces, low-power technology, and FPGA core architecture to offer new capabilities with its 40-nm devices.

The capability of 40-nm products also illuminates which applications will most significantly benefit here. With up to 48 transceivers, hard IP support for PCI Express (Gen1 and Gen2, x1–x8), twice the density of any other FPGA family, faster performance (both core and I/O), and lower power than any prior generation, any customer design focused on leading performance while balancing power will see compelling advantages. These devices are on track to sample this year, which could provide a 12-month advantage for Altera customers.

Q. One of Altera's more unique offerings is the HardCopy ASIC. Tell us about this and about how it works with FPGA-based designs and possible transitions to ASICs.

A. Prototyping based on *Stratix* series FPGAs allows you to get your system and system software/firmware ready prior to *HardCopy ASIC* design handoff. One design, using one RTL, one set of IP cores, and one tool (*Quartus II* design software), delivers both FPGA and ASIC implementations. Since all test insertion is managed by the *HardCopy* Design Center, designers don't need to spend any time on design for test. In addition, designers spend zero time on design for manufacturability or design for yield. Altera's extensive design experience and solid, long-standing partnership with TSMC means excellent built-in manufacturability, yield, and reliability.

Q. Moving away from the "high end," tell us about Altera's lower end, more cost-sensitive FPGAs. Is there anything new there that developers might want to know about?

A. In the cost-sensitive segment, Altera continues to innovate and provide leading edge solutions. The zero-power *MAX IIZ CPLDs* are the newest addition to our *CPLD* series. Ideal for portable and other power-, space-, and price-constrained applications, *MAX IIZ* devices come in ultra-small packages with more logic and I/O resources than are offered by traditional macrocell-based *CPLDs* in the same package size.

In the FPGA arena, Altera's *Cyclone III* FPGAs offer an unprecedented combination of low power, high functionality, and low cost. In addition to strong customer adoption of these devices in the military, broadcast, and portable device market over the past year, Altera also now offers automotive-grade versions of the devices.

To assist designers new to FPGA-based processors, Altera offers the *Nios II Embedded Evaluation Kit, Cyclone III Edition*. The *Nios II* evaluation kit is a feature-rich, low-cost platform that provides a fast and simple "hands-on" way for embedded designers to assess the *Nios II* processor, SOPC Builder system design software, and their custom applications. Combining a *Cyclone III* Starter Board and a touch-screen LCD in a unique Plexiglas case, the *Nios II* evaluation kit allows developers to launch example applications, such as networking and audio and image processing, with the touch of a finger.

Altera continues to invest in the cost-sensitive portion of the market and will have new solutions to share in 2009.

Q. Finally, Altera is known for providing high-quality development tools and IP for your customers. Can you describe those for us, and if there is anything new for 2008/09, please share that.

A. The Altera *Quartus II* design software offers complete automated system definition and implementation, all without requiring lower-level HDL or schematics. The *Quartus II* software also is the only software from an FPGA vendor offering multiprocessor (e.g., the *Intel Core 2 Duo* and *Quad* and *AMD Athlon 64 X2*) support, taking advantage of today's dual- and quad-core computers.

Over the past five years, *Quartus II* software has consistently delivered the industry's fastest compile times for high-end FPGAs, averaging a 20 percent reduction annually. *Quartus II* software's incremental compilation feature offers users a second-to-none productivity advantage, capable of delivering up to a 70 percent compile-time reduction compared to a standard compilation.

Additional key features include:

- *SOPC Builder*: Offers support for incremental compilation and has key IP blocks in its design library, including JTAG and SPI interfaces.
- *MegaCore® IP Library*: Integrated in *Quartus II* software, allows users easy access to Altera's portfolio of IP cores, including PCI Express Gen2 hard IP.
- *TimeQuest timing analyzer*: Allows creation, management, and analysis of complex timing constraints as well as advanced timing verification.

Altera offers a broad portfolio of easy-to-use IP cores. These IP cores are high-quality “building blocks” that can be dropped into system designs, increasing productivity by avoiding the time-consuming task of creating complete designs from scratch. Altera's extensive IP portfolio includes communications and I/O interconnect technologies (such as Ethernet, PCI, PCI Express, and Serial RapidIO) and a broad range of cores for embedded systems and DSP applications.

Q. Thank you for this interview.