

INSIDERS' GUIDE: FPGAs, TOOLS, AND BOARDS



FEATURED INTERVIEW:

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ALDEC, INC.: ACTIVE-HDL 8.1 & NEW VERIFICATION TECHNOLOGIES

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Q. First of all, tell us a little bit about yourself and your responsibilities at Aldec.

A. I have 13 years of experience in High-Tech Marketing, working for Hewlett Packard, Micron and Aldec; 3 years in EDA. My primary responsibilities are to oversee all Marketing Activities for Aldec, including: PR, Editorial, Advertising, Webinar/Seminar/Training/Tradeshaw "Events", product management, UNITE EDA Partner Program Management, channel management, collateral development, and all standard business marketing functions.

Q. Before we talk a little about your new, *Active-HDL 8.1*, can you give us a very brief outline of Aldec. What is your "value proposition" for FPGA developers? What are the product offerings?

A. Aldec has been in the EDA business for 24 years offering HDL simulators & verification tools for the FPGA designer. Aldec tools offer high value, such as equivalent or better performance, more features and at an affordable price. Aldec offers a patented technology suite including: design entry, HDL simulators, co-simulation, design rule checking, hardware-assisted verification (emulator/accelerator/prototyping), co-verification, IP Cores, DO-254 compliance tool sets and engineering specialty solutions.

Q. Moving on to *Active-HDL 8.1*, this is a pretty big release for Aldec. What are its highlights?

A. Aldec is one of the first-to-market an FPGA simulator with full Assertions & Coverage support at an affordable price. *Active-HDL 8.1* supports SystemVerilog IEEE 1800 Assertions/Coverage, PSL & OVA. The product includes assertion & coverage viewer, breakpoint editor, code coverage viewer, advanced dataflow, assertion libraries, HDL editor and language assistant support.

Active-HDL 8.1 also includes enhanced support for VHDL 2008 (IEEE Standard P1076-2008) including new constructs and libraries. The new release supports new and updated libraries including: Assertions, OVL 2.2 and VTL. A new DPI-wizard to help create quick interfaces between SystemVerilog and C applications is now included in *Active-HDL 8.1*. The DPI-wizard allows simple entry of C/C++ tasks and functions and generates C wrappers, and sample SystemVerilog files. The wizard also creates a configuration file for compiling generated C files into a dynamic-link library.

Q. One feature that caught my eye in reviewing it, was the new *Code2Graphics™*. How does this work?

- A. The *Code2Graphics* converter is a tool designed for automatic translation of text sources into Active-HDL block and state diagrams. It analyzes VHDL, Verilog, or EDIF source files and generates one or more block diagram files depending on the number of design entities, modules, or cells found in the analyzed file. The *Code2Graphics* converter also translates a text description of a state machine written in VHDL or Verilog code into a flat or hierarchical state diagram.

Q. Another interesting feature is the linkage between Active-HDL and the Mathworks products, Simulink and Matlab. Tell us a little about what Mathworks users might get from this relationship.

- A. *Active-HDL 8.1* is one of the few FPGA simulators to provide a full co-simulation solution for DSP designs, which is included in our PE and EE *Active-HDL 8.1* configurations, unlike the competition who may not offer a solution at all or only as an “optional upgrade”.

MATLAB® users can benefit via the interface with *Active-HDL 8.1*, which allows scalar and array data exchange and built-in *MATLAB* command or M-file execution during HDL simulations in *Active-HDL*. The interface allows you to generate complicated stimulus in a testbench, describe functionality of some design units at a high level of abstraction, post-process simulation data (e.g. compute Fast Fourier Transform of the DSP block output) and visualize simulation data (statistical analysis, spectral analysis, etc.). *Active-HDL 8.1 MATLAB* interface is using the HDL simulator as primary verification environment, requesting *MATLAB* services from within VHDL or Verilog code. Unlike some competing solutions, this interface does not require additional *MATLAB* toolboxes, but can use them if they are available.

Simulink® users benefit from the interface to *Active-HDL 8.1*, by being able to place HDL black boxes directly on the *Simulink* diagram. Simple one-click procedure in *Active-HDL* generates M-file that is dropped into a black box, providing HDL model description and informing *Simulink* how to start *Active-HDL* during simulation. *HDL-Simulink* interface parameters such as type cast, precision, quantization and overflow handling are fully configurable from the *Simulink* diagram level. The interface allows Simulink users to keep their tool as test environment, enabling in-system verification of HDL components or even the entire HDL design. *Simulink* interface is further enhanced by support of other vendor blocksets (Altera DSP, Synplify DSP, Xilinx System Generator, etc.).

Q. A big development in the EDA space is the movement towards higher-level languages like SystemC or SystemVerilog, not to mention the whole “ESL” phenomenon. What new features exist to help developers follow this migration in EDA and make it “easy” or if not “easy,” “less painful?”

- A. First I’ll mention that we are seeing the adoption of SystemVerilog from several of our customers, a smaller percentage, are moving towards SystemC and the “ESL” higher level languages and methodologies. *Active-HDL 8.1* provides support for SystemVerilog verification methodologies and System-level verification solutions utilizing SystemC with its transaction-level models (TLMs).

SystemVerilog

Active-HDL 8.1 supports *IEEE 1800™* SystemVerilog, a unified hardware description and verification language and supports all three groups of constructs: design, assertions, and verification; most recent improvements were added in strings, classes and DPI areas. Future construct support, interoperable SystemVerilog verification methodologies, will include Open Verification Methodology (OVM) 2.0.

SystemC

Modeling the behavior of the entire system using a high-level language such as C, C++, or

MATLAB®, *Active-HDL 8.1* includes SystemC/C++ debugging, tracing source code, setting breakpoints, waveform viewing, watch/call stack viewing and total visibility in the design hierarchy, which is crucial for Electronic System Level (ESL) designers.

Q. I notice that Active-HDL 8.1 supports a PCB Interface, what are the Benefits of this integration for PCB designers?

- A. Yes, *Active-HDL 8.1* and the *CADSTAR* product from Zuken® provide an interface for robust and seamless PCB I/O pin conversion. Today's challenges with the FPGA to PCB flow is: I/O changes due to PCB constraints: Pin swapping, adjusting I/O properties, saving discrete component costs and I/O changes due to FPGA constraints: Timing, dedicated/special-purpose pins, voltage/termination compatibility and simultaneous switching outputs (SSO). *Active-HDL 8.1* and *CADSTAR* together solve these challenges. *Active-HDL* generates pin constraints file and integrates Synthesis, implementation and export/import of pin file to *CADSTAR* tools from its Design Flow Manager. Then, *Active-HDL* exports FPGA Pin information to *CADSTAR* PCB design editor and FPGA pin information is shared between FPGA and PCB design environments. For optimum Place and Route, PCB design require pin swapping. Pin swap in PCB requires updated file to be send back to *Active-HDL* to update the FPGA. *Active-HDL* imports SWAP Pin file and generates new constraints file for the FPGA Place and Route tool to update the FPGA. *CADSTAR* provides complete PCB design and layout tool set. Reads *Active-HDL* data (Pin File) and assigns pins for PCB design. Generates swap pin file for future constraints changes and optimizes routing pattern of the PCB design. The combined strength of Aldec *Active-HDL 8.1* and Zuken *CADSTAR*, provides a full system level design and verification environment delivering quality and reliability.

Q. In addition to Mixed-Language Simulation, Active-HDL 8.1 provides full Design Creation & Entry, what features does this include?

- A. *Active-HDL 8.1* provides design creation and entry on ALL configurations of *Active-HDL 8.1*. This subset of features includes: design entry, Block and State Diagram editing, waveform editor, stimulus generation, language assistant, templates and auto-complete, the Code2Graphics Converter, Macro/Tcl/Tk/Perl script support and legacy schematic design import and symbol import/export. These features are included in every shipping *Active-HDL 8.1* product/configuration.

Q. How much does the product cost? And can you point us to website URL's where a potential customer can learn about your products before buying? Are there webinars, tutorials, downloads, etc., that you would recommend?

- A. *Active-HDL 8.1* prices start at \$3,600 and go up from there - our prices are typically more affordable than the competition. *Active-HDL* is available in three Product Configurations - *Designer Edition (DE)*, *Plus Edition (PE)* and *Expert Edition (EE)*. The software is available in floating or node-locked configurations for the Windows operating system. Absolutely, below are the key product links to learn more about *Active-HDL 8.1*:

Active-HDL 8.1 Product Info: <http://www.aldec.com/activehdl/>

Active-HDL 8.1 Movies/Tutorials:

<http://www.aldec.com/Products/Movies.aspx?productid=ff724e4e-71f8-48db-bdf6-56f43fddf586>

Download Free Eval Version: <http://www.aldec.com/Downloads/default.aspx>

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Q. Thank you for this interview.